ELEKTOR ELECTRONICS

MB501L

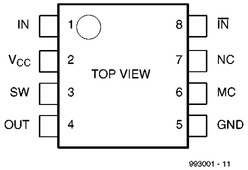
Integrated Circuits
Special Function, Prescalers

DATASHEET 1/99

MB501L
Two Modulus Prescaler

Manufacturer
Fujitsu. Internet: www.fujitsu.com

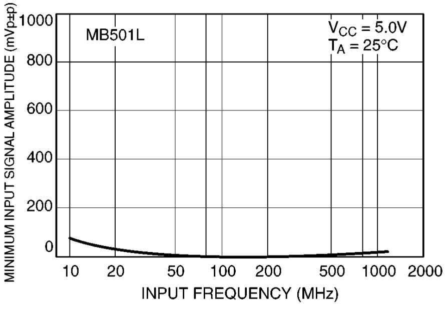
Application example
General Coverage Receiver,
Elektor Electronics January & February 1999



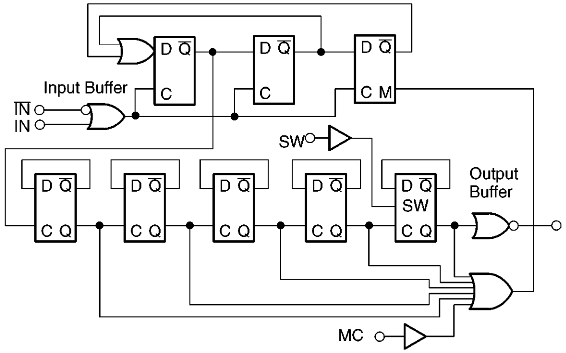
Pin assignment

Product Description
The Fujitsu MB501L is a two modulus prescaler used in a frequency synthesizer to make a Phase Locked Loop (PLL). It will divide the input frequency by the modulus of 64/65 or 128/129 The output level is 1.6V peak to peak on ECL level.

Features
- High Operating Frequency, Low Power Operation
  - 1.0 GHz at 150mW typ. (MB501)
  - 1.1 GHz at 50 mW typ. (MB501L)
- Pulse Swallow Function
- Wide Operation Temperature T_A = –40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{p-p}.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package



Input signal amplitude vs. input frequency



Block diagram

	SW	MC	Divide Ratio
MB501/501L	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}
L = GND to 0.8 V

ELEKTOR ELECTRONICS

AD8307

Integrated Circuits
Analogue

DATASHEET 1/99

AD8307
Low-Cost DC-500 MHz, 92 dB Logarithmic Amplifier

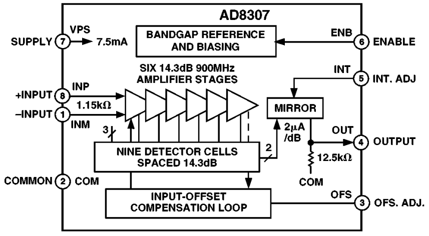
Manufacturer
Analog Devices, One Technology Way, P.O. Box 9106,
Norwood, MA 02062-9106, U.S.A.
Internet: www.analog.com.

Features
- Complete Multistage Logarithmic Amplifier
- 92 dB Dynamic Range: –75 dBm to +17 dBm To –90 dBm Using Matching Network
- Single Supply of 2.7 V Min at 7.5 mA Typical
- DC-500 MHz Operation, ±1 dB Linearity
- Slope of 25 mV/dB, Intercept of –84 dBm
- Highly Stable Scaling Over Temperature
- Fully Differential DC-Coupled Signal Path
- 100 ns Power-Up Time, 150 μA Sleep Current

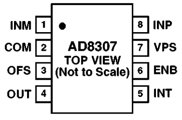
Applications
Conversion of Signal Level to Decibel Form
Transmitter Antenna Power Measurement
Receiver Signal Strength Indication (RSSI)
Low Cost Radar and Sonar Signal Processing
Network and Spectrum Analyzers (to 120 dB)
Signal Level Determination Down to 20 Hz
True Decibel AC Mode for Multimeters

Application Example
RF Decibel Meter, *Elektor Electronics* January 1999.

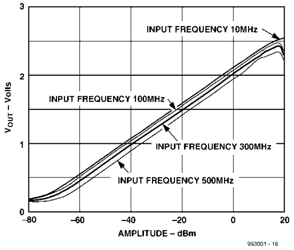
Product Description (excerpt)
The AD8307 is the first logarithmic amplifier in an 8-lead (SO-8) package. It is a complete 500-MHz monolithic demodulating logarithmic amplifier based on the progressive compression (successive detection) technique, providing a dynamic range of 92 dB to ±3 dB law-conformance and 88 dB to a tight ±1-dB error bound at all frequencies up to 100 MHz. It is extremely stable and easy to use, requiring no significant external components. A single supply voltage of 2.7 V to 5.5 V at 7.5 mA is needed, corresponding to an unprecedented power consumption of only 22.5 mW at 3 V. A fast-acting CMOS-compatible control pin can disable the AD8307 to a standby current of under 150 µA.



Functional block diagram



Pin configuration



V_{OUT} vs. input level (dBm) at various frequencies.

AD8307

Integrated Circuits
Analogue

DATASHEET 1/99

AD8307 Specifications (V_S = +5 V, T_A = 25ºC, RL ≥1MΩ, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
GENERAL CHARACTERISTICS					
Input Range (±1 dB Error)	Expressed in dBm re 50 Ω	–72		16	dBm
Logarithmic Conformance	f ≤100 MHz, Central 80 dB		±0.3	±1	dB
	f = 500 MHz, Central 75 dB		±0.5		dB
Logarithmic Slope	Unadjusted [1]	23	25	27	mV/dB
vs. Temperature		23		27	mV/dB
Logarithmic Intercept	Sine Amplitude; Unadjusted [2]		20		µV
	Equivalent Sine Power in 50 Ω	–87	–84	–77	dBm
vs. Temperature		–88		–76	dBm
Input Noise Spectral Density	Inputs Shorted		1.5		nV/√Hz
Operating Noise Floor	R_{SOURCE} = 50 Ω/2		–78		dBm
Output Resistance	Pin 4 to Ground	10	12.5	15	kΩ
Internal Load Capacitance			3.5		pF
Response Time	Small Signal, 10%-90%,0 mV-100 mV, C_L = 2pF		400		ns
	Large Signal, 10%-90%,0 V-2.4 V, C_L = 2 pF		500		ns
Upper Usable Frequency [3]			500		MHz
Lower Usable Frequency	Input AC-coupled		10		Hz
AMPLIFIER CELL CHARACTERISTICS					
Cell Bandwidth	–3 dB		900		MHz
Cell Gain			14.3		dB
INPUT CHARACTERISTICS					
DC Common-Mode Voltage	Inputs AC-Coupled		3.2		V
Common-Mode Range	Either Input (Small Signal)	–0.3	1.6	V_S–1	V
DC Input Offset Voltage [4]	R_{SOURCE} ≤ 50Ω		50	500	µV
	Drift		0.8		mV/ºC
Incremental Input Resistance	Differential		1.1		kΩ
Input Capacitance	Either Pin to Ground		1.4		pF
Bias Current	Either Input		10	25	mA
POWER INTERFACES					
Supply Voltage		2.7		5.5	V
Supply Current	V_{ENB} ≥ 2 V		8	10	mA
Disabled	V_{ENB} ≤ 1 V		150	750	µA

NOTES

[1] This may be adjusted downward by adding a shunt resistor from the Output to Ground. A 50 kΩ resistor will reduce the nominal slope to 20 mV/dB.

[2] This may be adjusted in either direction by a voltage applied to Pin 5, with a scale factor of 8 dB/V.

[3] See Application on 900 MHz operation.

[4] Normally nulled automatically by internal offset correction loop. May be manually nulled by a voltage applied between Pin 3 and Ground; see APPLICATIONS.

Specifications subject to change without notice.

MB501L

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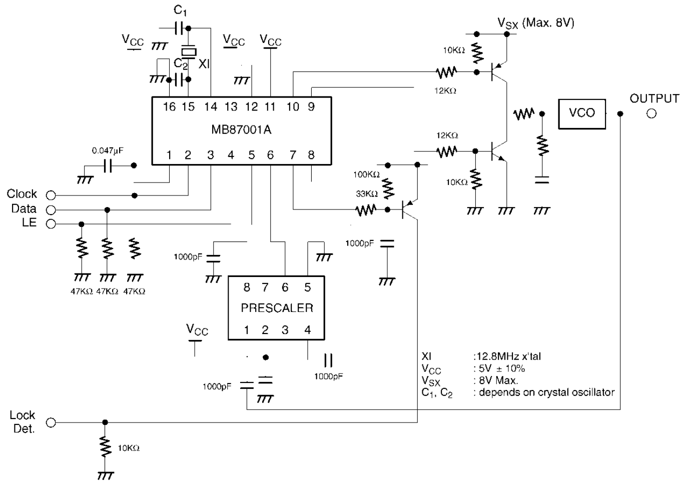
Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	ºC
Load Capacitance	C_L			12	pF



An example of application of MB501/501L/503/504/504L with PLL synthesizer IC MB87001A

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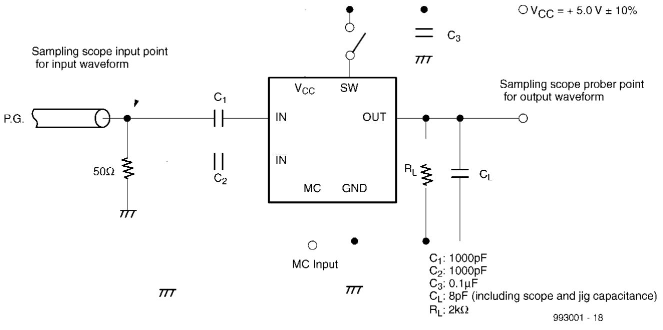
Typical application example


VCC = + 5.0 V ± 10%
C3
Sampling scope input point for input waveform
P.G.
C1
VCC
SW
IN
OUT
IN
MC
GND
Sampling scope prober point for output waveform
50Ω
C2
RL
CL
MC Input
C1: 1000pF
C2: 1000pF
C3: 0.1µF
CL: 8pF (including scope and jig capacitance)
RL: 2kΩ
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Test circuit